IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Farnsworth III, *et al.* Group Art Unit: 2138

Application No.: 10/651,874 Examiner: Tabone Jr, John J.

Filing Date: 08/29/2003 Docket No.: **BUR920030103US1**

Title: **PARTIAL GOOD INTEGRATED CIRCUIT AND METHOD OF TESTING SAME**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

OFFICE ACTION RESPONSE

Sir:

This communication is in response to the Office Action mailed March 28, 2007.